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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,512	08/10/2001	Hideto Ohnuma	12732-068001	4989

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,512	OHNUMA ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,11,14,18,21,32,33,35,36,52,53,55,58,65-78 and 86-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,14,21,33,36,53,58,72-78,93-99 and 103-117* is/are allowed.

6)☒ Claim(s) *1,11,18,32,35,52,55,65-71,86-92 and 100-102* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0606*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 87 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 87 recites the limitation "the diffraction grating pattern" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 86 and 88-91 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida, U.S. Patent 6,335,290.

Ishida shows the invention as claimed including a method of manufacturing a semiconductor device comprising the steps of: forming a conductive film 5 over a semiconductor 3 with an insulating film 4 therebetween; forming a resist pattern 7a over the conductive film by using one of a photomask and a reticle, wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the

resist pattern; and forming a gate electrode by etching using the resist pattern, wherein a thickness of an edge portion of the gate electrode is smaller than a thickness of a middle portion of the gate electrode (see figs. 1a-1d and col. 4-lines 18-67).

Concerning claim 88, note that the edge portion of the resist has a tapered configuration.

With respect to claims 89-90, note that the semiconductor is a semiconductor layer formed on an insulating surface and as broadly interpreted the semiconductor is a semiconductor substrate.

Regarding claim 91, note that the etching is dry etching (see col. 16-lines 1-8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 92 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida, U.S. Patent 6,335,290.

Ishida is applied as above but does not expressly disclose where the semiconductor device is part of one of the claimed electronic devices. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Ishida so as to include the semiconductor device in one of the claimed electronic devices because official notice is taken that the claimed electronic devices commonly have semiconductor devices such as the claimed device incorporated therein.

Claim 87 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida, U.S. Patent 6,335,290 in view of Yin, U.S. Patent 6,670,284.

Ishida is applied as above but does not expressly disclose wherein a plurality of slit portions are used as the diffraction grating pattern.

Yin discloses that it is well known in the art to perform photolithography processes using a diffraction grating (see col. 1-lines 28-42). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Ishida so as to conduct a photolithography process by a diffraction grating pattern because it is well known in the art that such a method can be utilized to form elements to be used in semiconductor devices.

Claims 1, 11, 18, 32, 35, 52, 55, 61, 65-71, 86-92, and 100-102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, EP 1 003 223 A2 in view of Ishida, U.S. Patent 6,335,290 and further in view of Yin, U.S. Patent 6,670,284.

Yamazaki shows the invention substantially as claimed including forming a conductive film 108 over a semiconductor 102 with an insulating film 103 therebetween; forming a resist pattern 109 on the conductive film; forming a gate electrode 108 by a first etching using the resist pattern wherein a thickness of an edge portion of the gate electrode is smaller than a thickness of a middle portion of the gate electrode; and introducing an impurity element into the semiconductor with the gate electrode as a mask to form a first impurity region and a second impurity region in the semiconductor 102, wherein the first impurity region is not overlapped with the gate electrode and the second impurity region is overlapped with the edge portion of the gate electrode (see figs. 1A-4D and paragraphs 0031-0073).

Yamazaki fails to expressly disclose wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern to form a tapered gate electrode, and forming a resist pattern by using one of a photomask having a diffraction grating pattern and a reticle having a diffraction grating pattern.

Ishida discloses wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern, and where the etching to form the tapered gate electrode is performed at least in part by dry etching (see fig. 1D, for example, and col. 4-lines 51-67, and col. 16-lines 5-8). In view of this

disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki shows as to form the tapered gate electrode as shown by Ishida because in such a way a step coverage of the device is improved.

Furthermore, Yin discloses that it is well known in the art to perform photolithography processes using a diffraction grating and a reticle over a photoresist material (see col. 1-lines 28-42). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Ishida so as to conduct a photolithography process by one of a photomask or reticle having a diffraction grating pattern because it is well known in the art that such a method can be utilized to form elements to be used in semiconductor devices.

Allowable Subject Matter

Claims 4, 14, 21, 33, 36, 53, 58, 72-78, 93-99, and 103-117 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard A. Booth
Primary Examiner
Art Unit 2812

July 24, 2006